GX1832 High-Accuracy Temperature Sensor With One-Wire

1 Features

- Direct Replacement for NTC Thermistors
- Accury: ± 0.5°C
- Supply Range: 2.6V ~ 5.5V
- Temperate Range: -55°C ~ +150°C
- Active Current: 40μA
- Shutdown Current: 0.5μA
- Resolution: 12 bits (0.0625°C)
- Interface: 1-Wire

2 Applications

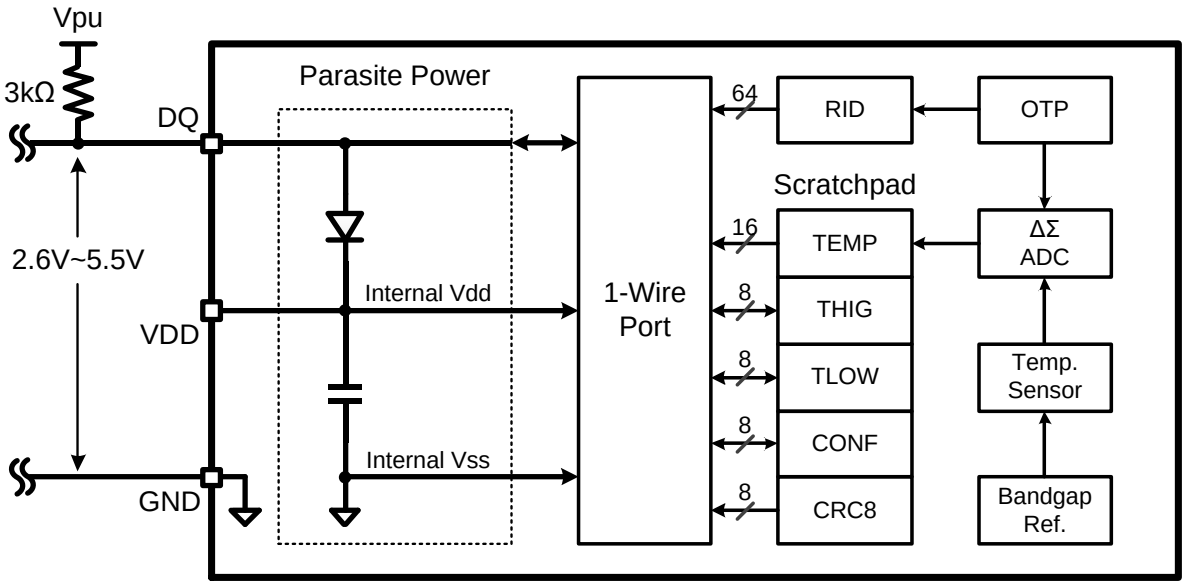
- Digital Output Wired Probes
- Industrial Control
- Cold-Chain Transportation
- Enterprise Servers

3 Description

The GX1832 is a fully integrated digital temperature sensor that provides a 12-bit temperature result with a resolution of 0.0625°C and an accuracy of up to ±0.5°C with no calibration.The GX1832 is compatible with the one-wire interface and supports up to 32 devices on a single bus. The GX1832 can be easily used as a two wire digital temperature probe or as a direct replacement for NTC thermistors.

Device Information

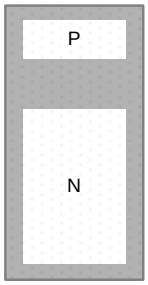
PART NUMBER	PACKAGE	BODY SIZE
GX1832D	DFN (2)	1.60 mm × 0.80
GX1832S	TO-92S (3)	4.00 mm × 3.00
GX1832WS	TO-92S-2 (2)	4.00 mm × 3.00
GX1832G	SOT23-3 (3)	2.90 mm × 1.30



Contents

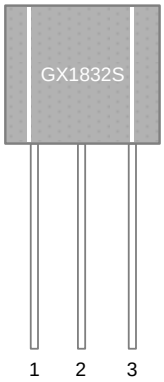
4 Pin Configuration

DFN-2



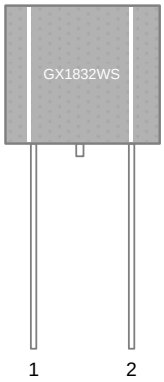
BOTTOM VIEW

TO-92S



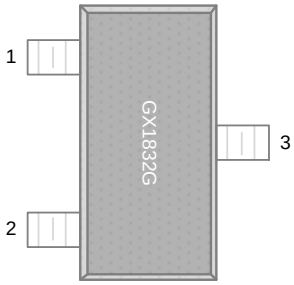
FRONT VIEW

TO-92S-2



FRONT VIEW

SOT23-3



TOP VIEW

PIN					DESCRIPTION
NAME	DFN-2	TO-92S	TO-92S-2	SOT23-3	
GND	N	1	1	3	Ground.
DQ	P	2	2	2	Data input/output.
VDD	-	3	-	1	Optional V_{DD}. Cannot connect to ground.

5 Specifications

5.1 Absolute Maximum Ratings

	MIN	MAX	UNIT
Input Voltage	- 0.5	6	V
Junction Temperature		150	°C
Storage Temperature	- 60	150	°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

5.2 ESD Ratings

		VALUE	UNIT
Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001-2017	± 6000	V
Latch-up	Latch-up (LU), per JESD 78F (2022)	± 200	mA

5.3 Electrical Characteristics

At T_A=-40°C~+125°C and V_{DD}=2.6V~5.5V, unless otherwise noted. Typical values at T_A=25°C and V_{DD}=3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	two wire (DQ to GND)	2.6	3.3	5.5	V
	three wire (VDD to GND)	1.4	3.3	5.5	V
Operating Temperature		- 55		150	°C
Temperature Accuracy	0°C to +85°C, 3.3V		± 0.3	± 0.5	°C
	- 40°C to 125°C		± 0.5	± 1	°C
Supply Sensitivity				0.1	°C/V
ADC Resolution			0.0625		°C
			12		bits
Conversion Time			26	35	ms
Quiescent Current	during conversion		40	80	μA
	during standby		0.5	3	μA
Pull-up Resistor		0.5	4.7	10	kΩ

6 Detailed Description

6.1 Temperature Output

The temperature data is stored as a 16-bit sign-extended two's complement number in the read-only temperature register, where 1 LSB=0.0625°C. When powered on or reset, the GX1832's temperature register is initialized to 0x0550 until the next temperature conversion is complete.

The users must enable the extended mode (EM=1) through the serial interface if the temperature range above 128°C needs to be measured. A specific example is shown in Table 1.

Table 1. Temperature Data Format

TEMPERATURE (°C)	NORMAL MODE (EM=0)	EXTENDED MODE (EM=1)
150	0x07FF	0x0960
128	0x07FF	0x0800
127.9375	0x07FF	0x07FF
125	0x07D0	0x07D0
85	0x0550	0x0550
75	0x04B0	0x04B0
50	0x0320	0x0320
25	0x0190	0x0190
0.25	0x0004	0x0004
0	0x0000	0x0000
–0.25	0xFFFC	0xFFFC
–25	0xFE70	0xFE70
–55	0xFC90	0xFC90

NOTE: Table 1 does not provide data formats for all temperatures.

6.2 Register Map

The GX1832 internal register stack consists of five registers, and the mapping is shown in Table 2. Table 3-11 describes the register contents.

Table 2. Register Map

BYTE	REGISTER	TYPE	RESET VALUE
1	Temperature	R	0x50
2		R	0x05
3	High Limit (T_H)	R/W	0x55
4	Low Limit (T_L)	R/W	0x00
5	Configuration	R/W	0x7F
6	CRC8	R	0xE3

LEGEND : R/W = Read/Write; R = Read only.

Table 3. Temperature Register (EM=0)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
Weight	sign	sign	sign	sign	sign	64	32	16	8	4	2	1	2^{-1}	2^{-2}	2^{-3}	2^{-4}
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND : R/W = Read/Write; R = Read only.

Table 4. Temperature Register (EM=1)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
Weight	sign	sign	sign	sign	128	64	32	16	8	4	2	1	2^{-1}	2^{-2}	2^{-3}	2^{-4}
Type	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

LEGEND : R/W = Read/Write; R = Read only.

Table 5. High Limit Register (EM=0)

BIT	7	6	5	4	3	2	1	0
Binary	H7	H6	H5	H4	H3	H2	H1	H0
Weight	sign	64	32	16	8	4	2	1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND : R/W = Read/Write; R = Read only.

Table 6. High Limit Register (EM=1)

BIT	7	6	5	4	3	2	1	0
Binary	H7	H6	H5	H4	H3	H2	H1	H0
Weight	sign	128	64	32	16	8	4	2
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND : R/W = Read/Write; R = Read only.

Table 7. Low Limit Register (EM=0)

BIT	7	6	5	4	3	2	1	0
Binary	L7	L6	L5	L4	L3	L2	L1	L0
Weight	sign	64	32	16	8	4	2	1
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND : R/W = Read/Write; R = Read only.

Table 8. Low Limit Register (EM=1)

BIT	7	6	5	4	3	2	1	0
Binary	L7	L6	L5	L4	L3	L2	L1	L0
Weight	sign	128	64	32	16	8	4	2
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND : R/W = Read/Write; R = Read only.

Table 9. Configuration Register

BIT	7	6	5	4	3	2	1	0
Binary	EM	-	-	-	-	-	-	-
Default	0	1	1	1	1	1	1	1
Type	R/W	R	R	R	R	R	R	R

LEGEND : R/W = Read/Write; R = Read only; - = Reserved.

Table 10. Configuration Register Field Descriptions

FIELD	DESCRIPTION
EM	Extended Mode EM=0: temperature range = −128°C ~ +127.9375°C. Out of range will clamp to +127.9375°C EM=1: temperature range = −256°C ~ +255.9375°C.

NOTE: The extended mode only changes the representation range and does not change the resolution.

Table 11. CRC8 Register

BIT	7	6	5	4	3	2	1	0
Binary	C7	C6	C5	C4	C3	C2	C1	C0
Default	1	1	1	0	0	0	1	1
Type	R	R	R	R	R	R	R	R

LEGEND : R/W = Read/Write; R = Read only;

NOTE: The CRC8 is generated based on the first five bytes of the register stack.

6.3 Serial Interface

6.3.1 Bus Overview

The 1-Wire bus is a single-master, multi-slave communication system implemented using only one signal line. All slaves on the bus need to drive the bus at appropriate times, so they must be loaded onto the bus in the form of open-drain outputs. The 1-Wire bus has a two-level command architecture consisting of addressing commands and function commands. Among them, addressing commands are generally used universally among different types of devices and are mainly used to select a specific slave on the bus for subsequent function commands; while function commands differ from one device type and application. The addressing commands supported by GX1832 are listed in Table 12, and the function commands are listed in Table 13.

All data and commands transmitted on the 1-Wire bus follow a transmit order of least significant bit (LSB) first.

Table 12. Addressing Commands

COMMAND	DESCRIPTION
0xF0	Search RID
0xEC	Alarm Search RID
0x33	Read RID
0x55	Match RID
0xCC	Skip RID

Table 13. Function Commands

COMMAND	DESCRIPTION
0x44	Convert
0xBE	Read Scratchpad
0x4E	Write Scratchpad

6.3.2 Node Address

GX1832 has a unique 64-bit RID in the 1-Wire bus used as a node address. As shown in Table 14, the lowest 8 bits are the family code of GX1832; the middle 48 bits are the serial number, and GXCAS supports customizing 32 different serial numbers; the highest 8 bits are the checksum of the family code and serial number.

Table 14. Node Address (RID)

BIT	[63:56]	[55:8]	[7:0]
Binary	CRC8	Serial Number	Family Code
Value	Calculated	Unique	0x29

6.3.3 Signal Timing

The 1-Wire bus defines the following six fundamental signal types: reset pulse, response pulse, read 0 time slot, read 1 time slot, write 0 time slot, and write 1 time slot. Except for the response pulse, all signals are initiated by the master and are counted from the falling edge of the bus.

The initialization sequence consisting of a reset pulse followed by a response pulse is a necessary starting step for all communication on the 1-Wire bus, as shown in Figure 1. The master sends a reset pulse by pulling the bus low for 480 us. The GX1832 recognizes the reset pulse and resets its communication state, then sends a response pulse. To detect the response pulse, the master must sample the bus within a specific window time. When the sampled bus is at a logic low, it indicates the presence of a response pulse, indicating that the GX1832 is ready to start communication; when the sampled bus is at a logic high, it indicates the absence of a response pulse, indicating that the reset pulse was not recognized by the GX1832 or that no GX1832 is attached to the bus. For maximum timing margin, GXCAS recommends sampling the bus at 70us.

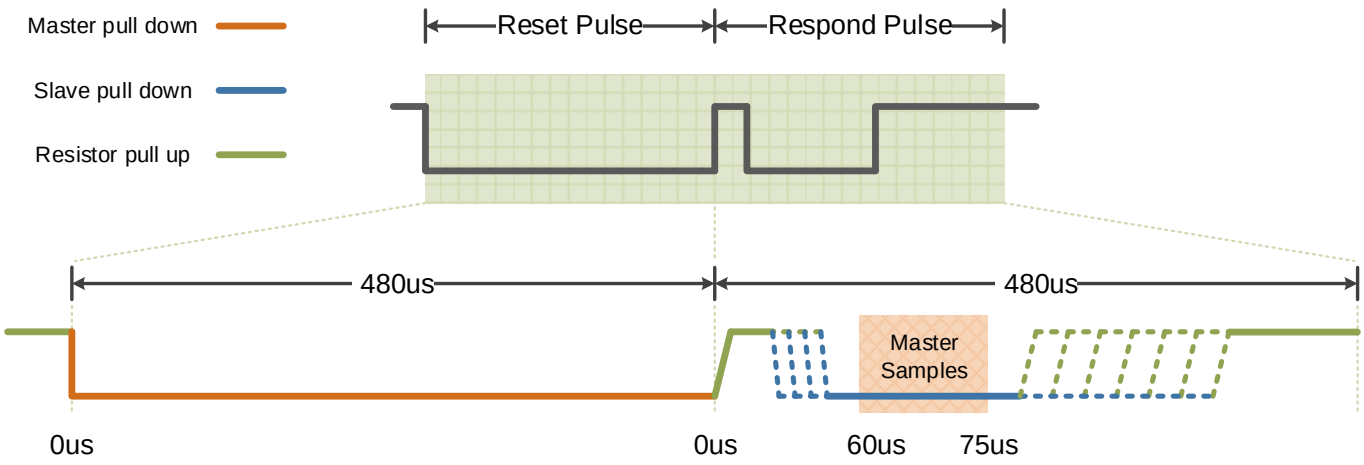


Figure 1. Initialization Sequence

1-Wire data transmission operates in time slots, each carrying only one bit of data. In this system, write slots transmit data from the master to the slave, while read slots transmit data from the slave to the master. Both write and read slots begin with the master pulling the bus low. As shown in Figure 2, the width of each time slot is not less than 65us; a recovery time of at least 1us must be provided between adjacent time slots. Together, these specifications limit the maximum possible communication rate of the 1-Wire bus to 15kbps.

The GX1832 is capable of transmitting data to the master only when the master initiates a read slot. The master should pull the bus low for at least 1us to ensure that the bus falling edge is recognized by the GX1832. If successful recognition occurs, the GX1832 will determine its subsequent operation on the bus based on the data it is about to send. Therefore, two types of signals can be further distinguished within the read slot.

- Read 0 Slot : From the bus falling edge, the slave pulls the bus low for 15 to 60us;
- Read 1 Slot : From the bus falling edge, the slave releases the bus directly.

In order to receive the data transmitted by GX1832, the master must sample the bus within a specific window time. The sampling result is the received one bit of data. Considering the maximization of the timing margin, GXCAS recommends releasing the bus at 5us and sampling the bus at 15us.

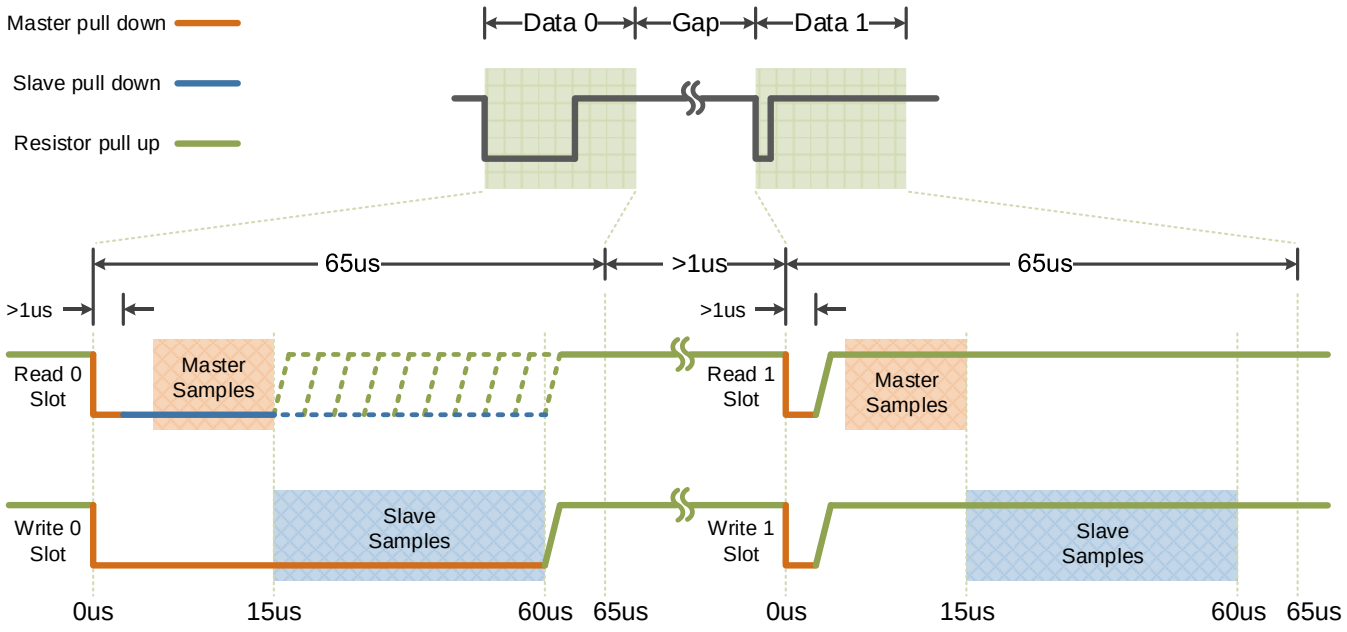


Figure 2. Read/Write Slot

The master initiates a write slot to send data to the GX1832. The master should pull the bus low for at least 1us to ensure that the bus falling edge is recognized by the GX1832. If successful recognition occurs, the GX1832 will sample the bus within a specific window time, and this sampling result represents the received data bit. Therefore, the write slot can be further divided into two signals:

- Write 0 Slot : The master should pull the bus low for at least 60us;
- Write 1 Slot : The master should release the bus within 15us.

6.3.4 Communication Process

After GX1832 is powered on, it takes approximately 3ms to stabilize, during which any communication operation is prohibited. The subsequent communication process unfolds as follows:

Step-1: The master issues the initialization sequence;

Step-2: The master issues the addressing command and performs essential data exchange;

Step-3: The master issues the function command and performs essential data exchange.

Users are required to strictly adhere to the prescribed communication flow. Any omissions or deviations from the specified sequence of steps will result in non-responsiveness from GX1832. The complete communication flow is illustrated in Figure 3. The only exception occurs when the search command (0xF0 and 0xEC) is utilized during the search process, allowing the master to bypass Step-3.

After the completion of the initialization sequence, the master is able to transmit an addressing command for selecting a specific slave. The GX1832 is compatible with the following five addressing commands.

● Search RID [0xF0]

When the system is initially activated, the master must ascertain the RIDs of all connected slaves on the bus to verify their type and quantity. The 1-Wire bus employs an elimination method to determine the RIDs of the slaves, necessitating multiple search procedures in a loop for traversing all connected slaves on the bus.

The search process comprises a search command and the necessary exchange of data. Data exchange commences with the least significant bit of the RID. For each bit of the RID, the master must continually initiate three slots. In the first slot, participating slave devices transmit their true values of the RID for that bit; in the second slot, they transmit their inverted values of the RID for that bit. Due to the wire-AND characteristic of the open-drain structure, the bus output value is determined by performing a bitwise AND operation on all values transmitted by slaves. This implies that different information can be expressed through four distinct cases.

- TRUE=0, INV=0: The slaves participating in the search have a RID difference at this bit position;
- TRUE=0, INV=1: The slaves participating in the search have their RID bits set to 0 at this position;
- TRUE=1, INV=0: The slaves participating in the search have their RID bits set to 1 at this position;
- TRUE=1, INV=1: Bus failure, or removal of a slave during the search process.

The master is required to determine the selection value based on the readout results of the initial two time slots and transmit it during the third time slot. Any RIDs belonging to slaves with a selection value differing from that of the master will be excluded from subsequent search processes. This entire procedure is iterated 64 times, ultimately leading to the identification of one RID associated with a slave on the bus. Repetition of this process enables identification of all slaves present.

- Alarm Search RID [0xEC]

This command is functionally equivalent to the search RID command (0xF0), except that it only involves slaves with the ALARM flag set. Following a temperature conversion by GX1832, if the resulting temperature falls beyond the user-defined high and low alarm threshold values, the ALARM flag will be activated.

- Read RID [0x33]

This command directly retrieves the 64-bit RID from the slave device. When there is only one slave device on the bus, this command can more accurately identify its RID. However, if multiple slaves are connected to the bus, all slaves will simultaneously transmit their RIDs, leading to a data collision on the bus. Users should take precautions to avoid this scenario.

- Match RID [0x55]

This command necessitates the inclusion of the anticipated 64-bit RID. Only the slave possessing an identical RID will execute the subsequent function command.

- Skip RID [0xCC]

The command selects all the slaves on the bus directly. When combined with the temperature conversion command (0x44) or write scratchpad command (0x4E), it enables global access functionality, allowing simultaneous operation of all slaves. However, this command cannot be used in conjunction with the read scratchpad command (0xBE) as it would result in a bus data collision caused by simultaneous transmission of data from all slaves. Users should avoid this scenario.

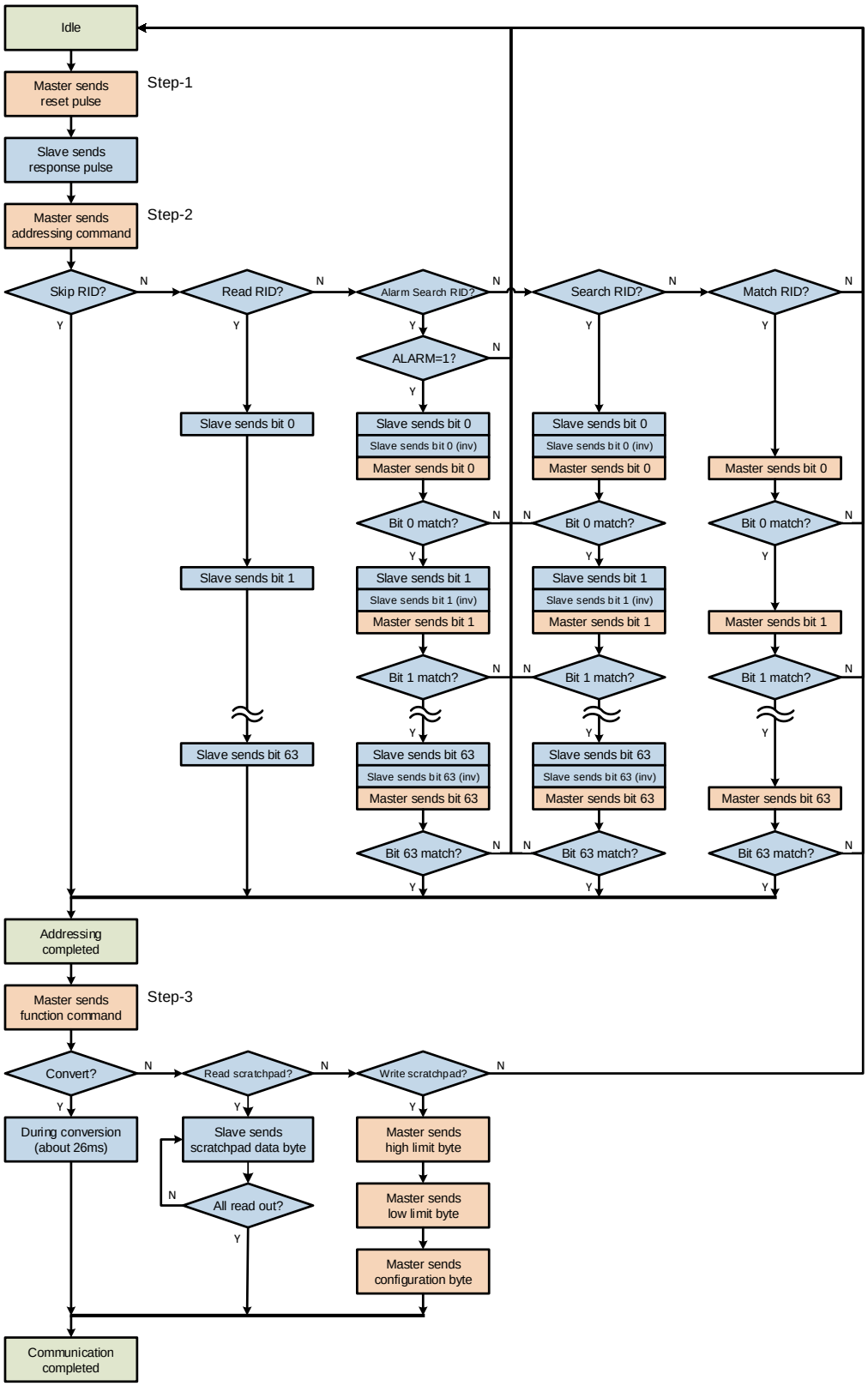


Figure 3. Flowchart for Communication

The addressed slave is capable of receiving and executing subsequent function commands. The GX1832 supports the following three function commands.

- Convert [0x44]

This command triggers a temperature conversion and stores the measured temperature in a read-only register. In comparison to the DS18B20, the GX1832 exhibits significantly lower power consumption during conversion, eliminating the need for a strong pull-up condition from the master. However, it is crucial to allow sufficient time for the conversion to complete before initiating communication with the GX1832 to avoid potential impact on measurement accuracy. In a two-wire connection, failure to do so may even result in chip reset due to power outage.

- Read Scratchpad [0xBE]

This command enables the master to access the entire scratchpad of the GX1832. Data transfer commences with the least significant bit of byte 1 and concludes with the most significant bit of byte 6. If only a portion of the cache area is required, the master can initiate a reset pulse at any time to terminate subsequent read operations.

- Write Scratchpad [0x4E]

This command enables the master to modify the partial scratchpad of the GX1832. Data transmission commences from the least significant bit of byte 3 and concludes at the most significant bit of byte 5. Data is stored in the scratchpad in byte units. If a reset pulse is sent by the host midway through a byte, the data for that byte will be lost.

6.3.5 Cyclic Redundancy Check

The GX1832 conducts cyclic redundancy check (CRC) on both RID and scratchpad data, as illustrated in Table 15 below. The generator is depicted in Figure 4. The master should recalculate the CRC value and compare it with the received CRC value to validate the integrity of the data read from GX1832.

Table 15. CRC-8 Rule

RULE	ATTRIBUTES	RULE	ATTRIBUTES
CRC width	8-bits	Input data reflected	False
CRC polynomial	$x^8 + x^5 + x^4 + 1$ (0x31)	Output data reflected	False
Initial seed value	0x00	XOR value	0x00

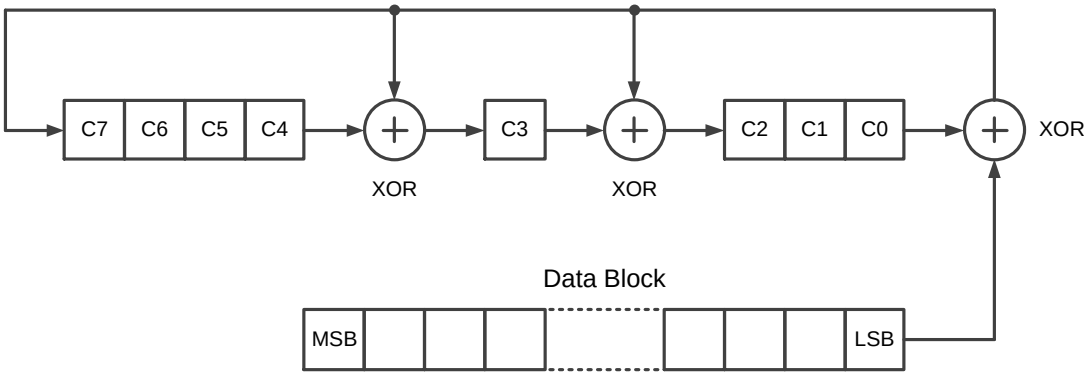


Figure 4. CRC-8 Generator

6.4 Power Mode

6.4.1 Parasite Power Mode

When utilizing a two-wire connection, the GX1832 operates in parasitic power mode. During high logic level on the bus, the GX1832 draws current from the bus to power its internal modules. Conversely, during low logic level on the bus, the GX1832 utilizes stored charge in its large internal capacitor to power its internal modules. A diode is employed to prevent reverse leakage of capacitor charge during communication. The schematic diagram of the parasitic power supply connection is depicted in Figure 5. GXCAS does not recommend the use of parasite power mode for high-temperature applications (>125°C) due to the significant leakage current in semiconductor devices at elevated temperatures, which may result in the inability to maintain normal communication.

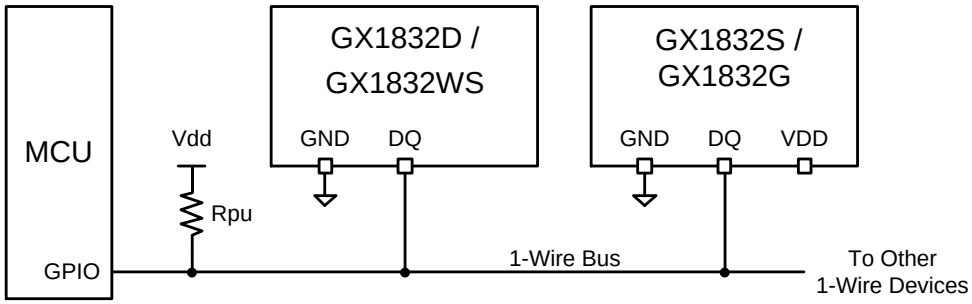


Figure 5. Powering the GX1832 without an External Supply

6.4.2 External Power Mode

Only the GX1832S and GX1832G are capable of being connected with three wires and operating in external power mode, as illustrated in Figure 6. In this scenario, the minimum operating voltage can be reduced to 1.4V.

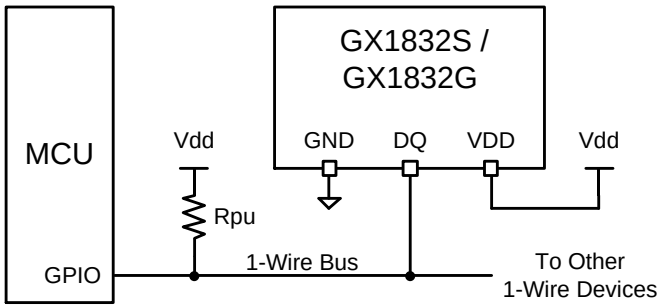


Figure 6. Powering the GX1832 with an External Supply

7 Application and Implementation

NOTE

The following contents are precautions for the use of GX1832 in specific applications. GXCAS does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 High-Temperature Application

For high-temperature applications (>125°C), GXCAS recommends using GX1832S or GX1832G with an external power supply. It is not recommended to use GX1832D or GX1832WS. GXCAS only ensures the high-temperature characteristics of GX1832D and GX1832WS through design, rather than factory testing. Users have three options to reduce the impact of high temperature on parasitic power mode.

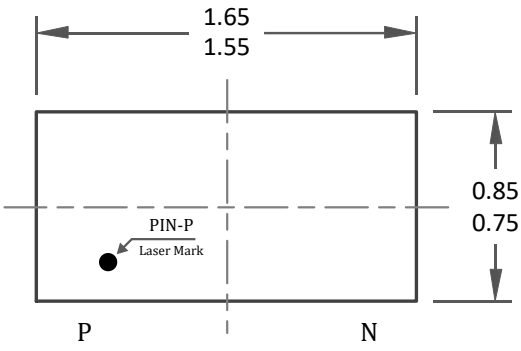
- Place a capacitor of more than 10uF between the power pin and the ground pin.
- Consider increasing the supply voltage and using a pull-up resistance of less than 3kΩ.
- Reduce the reset pulse duration to 300us and extend the recovery time between adjacent slots to 30us.

7.2 Layout Guidelines

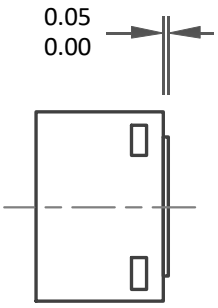
The GX1832 should be isolated from sources of noise, such as high-speed digital buses, coil elements, and wireless antennas. When using a three-wire connection, GXCAS recommends the placement of a low-ESR ceramic capacitor between the power pin and ground pin to effectively filter out power noise. The capacitor should be positioned as close to the power pin as possible, with a recommended value of 0.1uF.

8 Package Information

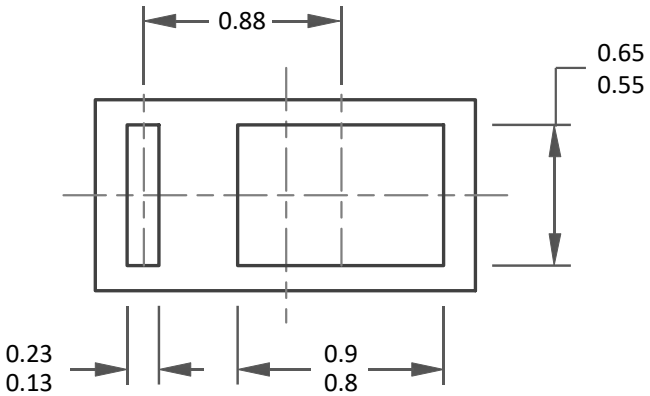
8.1 Package Outline (DFN-2)



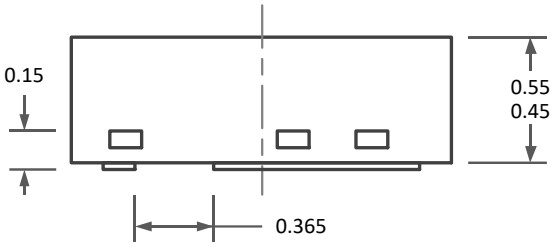
TOP VIEW



SIDE VIEW

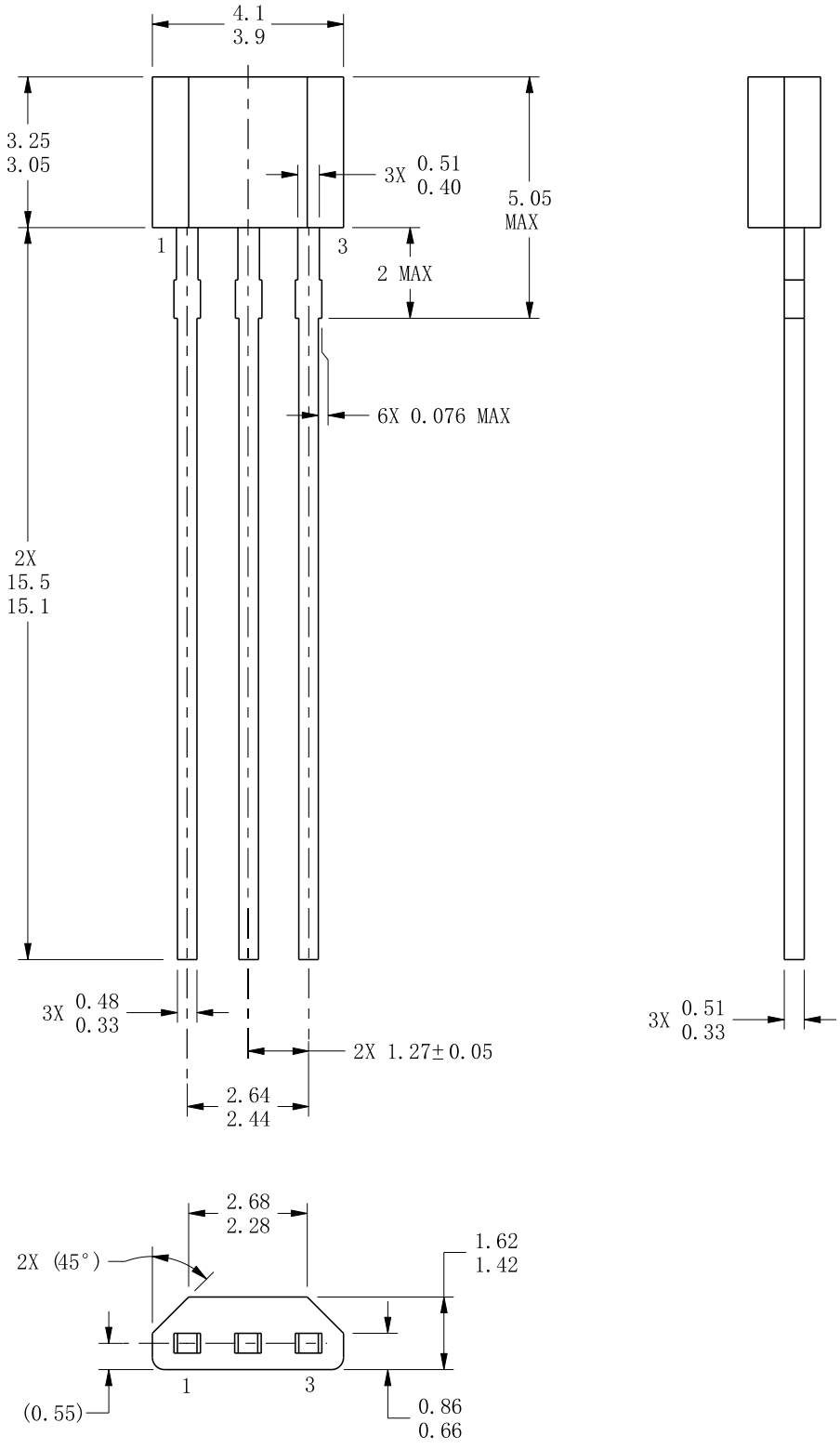


BOTTOM VIEW

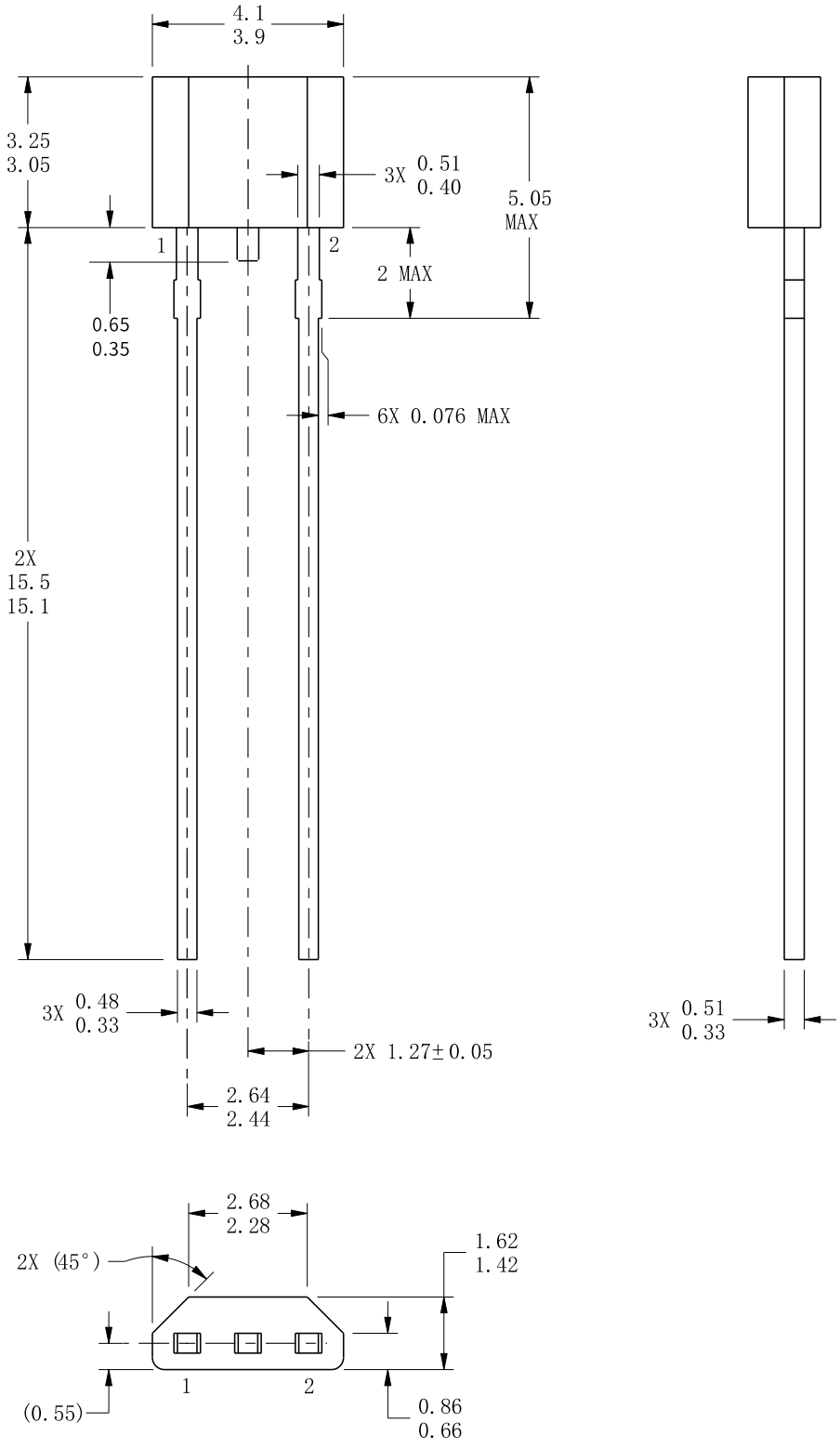


SIDE VIEW

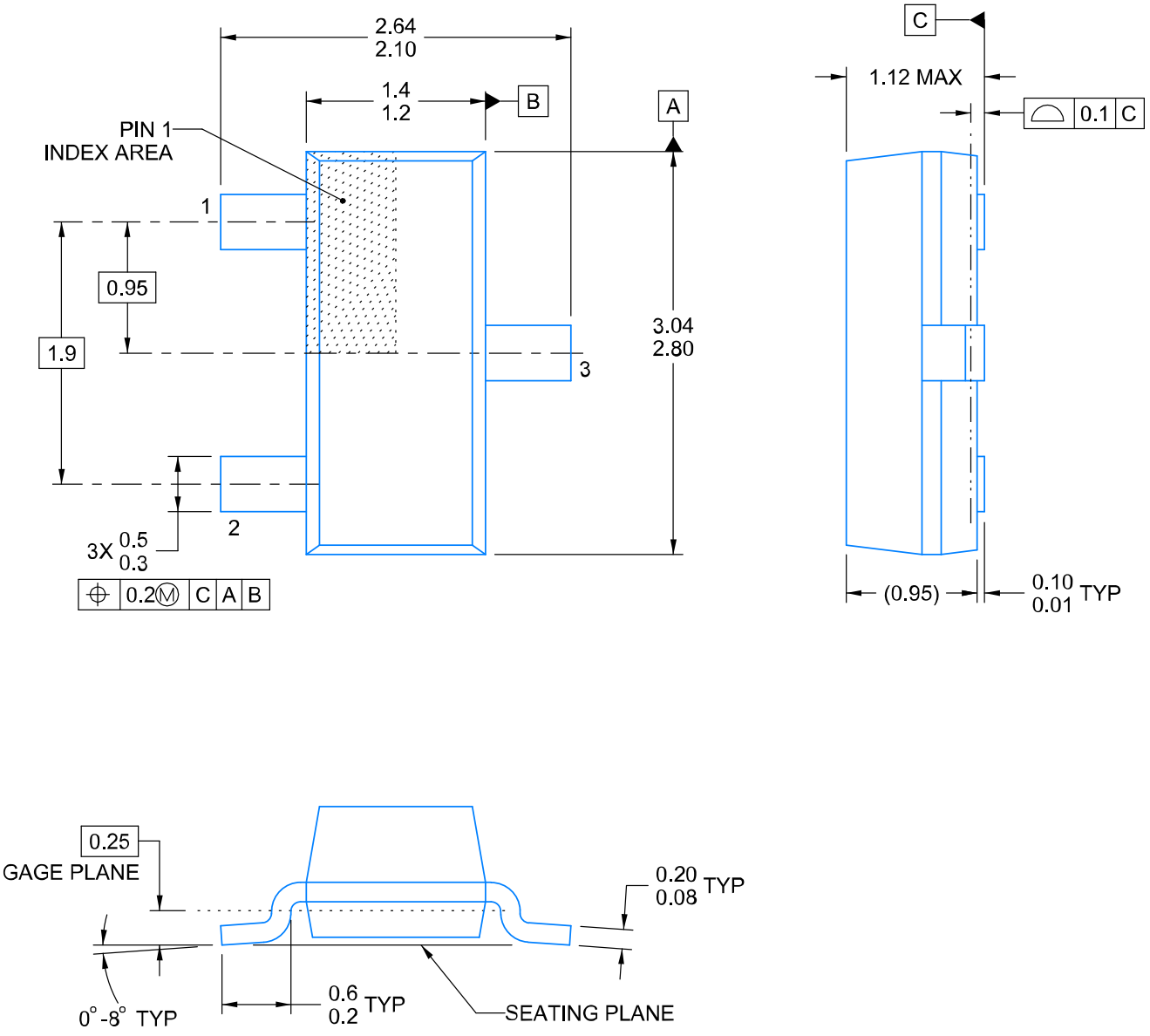
8.2 Package Outline (TO-92S)



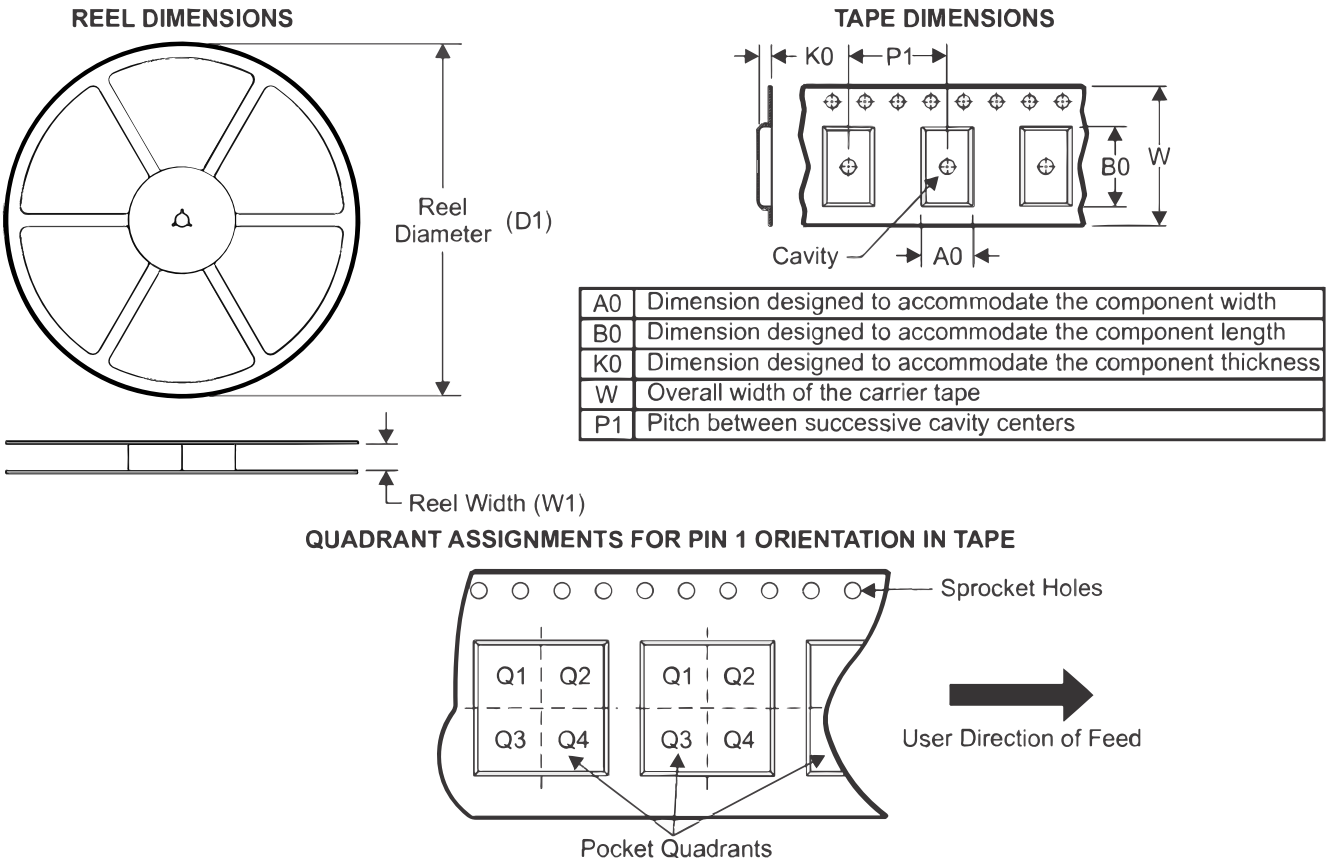
8.3 Package Outline (TO-92S-2)



8.4 Package Outline (SOT23-3)



8.5 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

PACKAGE	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	PIN1
DFN	180	8.6	1.00	1.80	0.62	4.00	8.00	Q1
SOT23	178	9.5	3.15	2.77	1.22	4.00	8.00	Q3

Note : all of the above dimensions are in millimeters.

9 Order Information

ORDER PN	DEVICE	PACKAGE	SPQ	REMARK
GX1832Dx-T&R	GX1832Dx	DFN (2)	4000	tape and reel
GX1832Sx-Bu	GX1832Sx	TO-92S (3)	2000	bulk
GX1832WSx-Bu	GX1832WSx	TO-92S-2 (2)	2000	bulk
GX1832Gx-T&R	GX1832Gx	SOT23-3 (3)	3000	tape and reel

Note: The "x" in the order PN denotes 32 distinct serial numbers.

10 Rivision History

VERSION	DATE	CONTENT	PAGE
V0.0	2023-7	First draft	-
V1.0	2023-8	Added package information and order information	18~21
V1.1	2023-10	Added SOT23-3 package	21~22